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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
DANG, KHANH	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JACK B. DENNIS and SAM B. SANDBOTE

Appeal 2007-4334
Application 09/715,772
Technology Center 2100

Decided: July 28, 2008

Before JAMES D. THOMAS, ST. JOHN COURTENAY III, and THU A. DANG, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-41. We have jurisdiction under 35 U.S.C. § 6(b). An Oral Hearing regarding this appeal was conducted on July 9, 2008.

We AFFIRM.

THE INVENTION

The disclosed invention relates generally to computer architecture (Spec. 1). More particularly, Appellants' invention is directed to multi-thread computers (*Id.*)

Independent claim 1 is illustrative:

1. An apparatus comprising:

a peripheral bus coupled to a peripheral unit to transfer peripheral information including a command message specifying a peripheral operation; and

a processing slice coupled to the peripheral bus to execute a plurality of threads comprising instructions, the plurality of threads including a first thread sending the command message to the peripheral unit;

wherein the processing slice comprises a functional unit to perform a register operation specified in the instructions dispatched from each of the plurality of threads; and

wherein the processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle.

THE REFERENCES

The Examiner relies upon the following references as evidence in support of the rejections:

Hiraoka	US 5,418,917	May 23, 1995
Motomura	US 5,815,727	Sep. 29, 1998

Dove US 5,938,765 Aug. 17, 1999

THE REJECTIONS

1. Claims 1-12, 14-25, 27-38, and 41 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Motomura.
2. Claims 13, 26, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Motomura in view of Hiraoka.
3. Claim 40 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Motomura in view of Hiraoka and Dove.

CLAIM GROUPING

> When multiple claims subject to the same ground of rejection are argued as a group by appellant, the Board may select a single claim from the group of claims that are argued together to decide the appeal with respect to the group of claims as to the ground of rejection on the basis of the selected claim alone. Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.

37 C.F.R. § 41.37(c)(1)(vii) (2006).[1]

Regarding the anticipation rejection of claims 1-12, 14-25, 27-38, and 41, Appellants argue claims 1-7, 10-12, 14-20, 23-25, 27-33, 36-38, and 41

[1] We cite to the version of the Code of Federal Regulations in effect at the time of the Appeal Brief. The current version includes the same rules.

as a first group (App. Br. 10-14), and claims 8, 9, 21, 22, 34, and 35 as a second group (App. Br. 14-16).

We select independent claim 1 as the sole claim on which to decide the appeal of the first group, and dependent claim 8 as the sole claim on which to decide the appeal of the second group. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Regarding the obviousness rejection of claims 13, 26, and 39 that stand rejected as being unpatentable over Motomura in view of Hiraoka, we consider each of claims 13, 26, and 39 separately, as argued in the Brief (pp. 16-17).

We consider the obviousness rejection of claim 40 as being unpatentable over Motomura in view of Hiraoka and Dove separately, as argued in the Brief (pp. 17-18).

PRINCIPLES OF LAW

Anticipation under 35 U.S.C. § 102

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.,* 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

ANALYSIS

Independent claim 1

We consider the Examiner's rejection of representative claim 1 as being anticipated by Motomura. Appellants present the following principal arguments on appeal:

Appellants note that because each processor 110 shown in Motomura's Figure 1 "can only execute one thread at a time, it is necessary to consider the entire parallel processor system (Motomura, Fig 1, element 100) as the processing slice, as the Examiner concedes." (App. Br. 12, ¶1). Appellants contend that "[i]f the parallel processor system of Motomura is equivalent to a processing slice in Appellants' claim 1, then there is no analogous 'peripheral unit' disclosed in Motomura, as the alleged 'peripheral unit' (the ordered multithread executing system) would therefore be contained within the processing slice of claim 1."

In response, we note that during the oral Hearing conducted on July 9, 2008, Appellants' representative Edward J. Kessler acknowledged that it was reasonable that a peripheral unit was inherently coupled to the parallel processor system of Motomura (*see* Record of Oral Hearing Transcript, p. 12, lines 4-23). We agree.

See Record of Oral Hearing Transcript, p. 12, lines 4-23:

> JUDGE COURTENAY: Are you conceding that the reference inherently has a peripheral and a peripheral BUS?

MR. KESSLER: I will say that, yes, it would probably -- you would need a peripheral BUS in order to have an operative system.

JUDGE COURTENAY: So you are conceding that point?

MR. KESSLER: It doesn't disclose it, but, yes, you would need one.

JUDGE COURTENAY: So inherently, you agree that the reference necessarily has a peripheral BUS and a peripheral to meet the limitation of your claim? You agree or disagree? The Examiner appears to be making an inherency argument.

MR. KESSLER: Right. Right. I agree with that. And --

JUDGE COURTENAY: But at the same time, the Examiner is reading the processing slice on the entirety of Figure 1 of the reference.

MR. KESSLER: Yeah. And yes, there would be a peripheral BUS that would hang off of that entirety of the reference.

JUDGE COURTENAY: So you're not contesting that limitation with your claim?

MR. KESSLER: Not really.

JUDGE COURTENAY: Okay.

MR. KESSLER: I'm not going to strongly contest it, no.

Appellants further contend that Motomura does not disclose the claimed "functional unit," as follows:

> Assuming, ***arguendo,*** that the sum total of processors disclosed in Motomura are analogous to a single processing slice as in claim 1, the Examiner's rejection nonetheless fails for want of a "functional unit", which under the Examiner's present scenario is analogous to a single processor in Motomura.

(App. Br. 12, ¶3).

During prosecution, "the PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)).

We begin our analysis by construing the scope of the claimed "functional unit." When we look to Appellants' Specification for *context*, we find the operation of the claimed "functional unit" described as follows:

> The functional unit 450 performs an operation specified in the dispatched instruction. The functional unit 450 performs all operations of the instruction set that manipulate values in the data registers. These operations include arithmetic and logical register operations, shift and selected bit operations. The operation performed by the functional unit 450 is determined by a decoded opcode value passed from the instruction decoder and dispatcher 416. The functional unit 450 has connections to the condition code memory 440 to set a thread's condition code according to the outcome of an arithmetic operation or comparison.

(Spec. 12, 5-12).

We also note that Appellants' Specification further discloses that "[t]he processing slice includes an instruction processing unit, a thread

control unit, a peripheral unit, a memory access unit, *a functional unit*, a condition code memory, and a register file. The processing slice is configured to support execution of a number of threads." (Spec. 4:27 – 5:2).

Here, we decline to read limitations recited in the Specification into the claim. *See E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1369 (Fed. Cir. 2003) (Limitations appearing in the specification but not recited in the claim are not read into the claim). Instead, we broadly but reasonably construe the claim term "functional unit" as any unit that is capable of performing the claimed function of performing a register operation specified in the instructions dispatched from each of the plurality of threads (claim 1).

After considering the record before us, we note that the Examiner is reading the claimed "processing slice" on Motomura's parallel processor system 100 (Ans. 15, ¶3). The Examiner is also reading the claimed "functional unit" on Motomura's processor(s) 110 (*Id.*). Both of these elements are shown in Motomura's Figure 1.

As a preliminary matter, we note that all computer processors include internal registers that perform operations when instructions are fetched and executed. Thus, we find that Motomura's plurality of processors 110 (col. 8, ll. 2-3, Fig. 1) provide a structure (i.e., a functional unit) that is clearly capable of performing the claimed function of performing a register operation specified in the instructions dispatched from each of the plurality of threads (claim 1). Our reviewing court has determined that the absence of a disclosure relating to function does not defeat a finding of anticipation if

all the claimed structural limitations are found in the reference. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997).

Here, we find that the claimed structural limitations are found in the reference (i.e., a plurality of processors 110 corresponding to the claimed "functional unit"). See also Motomura's disclosure of processor 110 executing a thread at column 8, lines 26-27.

Appellants further contend that Motomura does not disclose the claimed functional limitations of executing instructions from more than one of a plurality of threads concurrently in a clock cycle:

> Appellants' claim 1 and Motomura are very different. Appellants' claim 1 recites executing "instructions from more than one of the plurality of threads concurrently in a clock cycle." In Motomura, each processor can execute only one thread at a time, as it is disclosed that each thread must go into a "waiting" or "completed" state before another thread is assigned to the processor. (Motomura, col. 8, 11. 40-51). In contrast, Appellants' specification supports the claim language by disclosing that "[e]ach of the [processing slices] operates by interleaving the execution of instructions from the four threads, including the ability to execute several instructions concurrently in the same clock cycle." (Specification, p. 8, 11. 23-25).

(App. Br. 11).

We agree with Appellants' statement that each of Motomura's processors 110 is only capable of single-threaded operation. In particular, the multiple references in column two of Motomura to a "sequential execution path" support this finding. (*See e.g.,* col. 2, l. 2). We also find no

explicit mention of a clock signal in the Motomura reference. Nevertheless, we find that each of Motomura's processors 110 must (i.e., inherently) be clocked to be operational (Motomura, Fig. 1). We note agreement with Appellants' representative on at least this point:

See Record of Oral Hearing Transcript, p. 8, lines 15-20:

> JUDGE COURTENAY: I did a text search of the reference and I could not find the terms "clock" or "cycle" in the entirety of the reference. And I'm looking at the figures. I don't see a clock, although I think most people would agree that a clock is inherent in any computer or processor system. You have to have a clock to drive the processor.
>
> MR. KESSLER: I agree.

Thus, we find that Motomura teaches a structure (i.e., a processing slice) that includes of a plurality of single-threaded processors, each of which is necessarily clocked. More particularly, we find that Motomura teaches a structure (i.e., a "processing slice" that includes a plurality of single-threaded processors 110) that is capable of performing the recited functional language of "execut[ing] the instructions from more than one of the plurality of threads concurrently in a clock cycle," (claim 1) because the plurality of processors 110 (each of which is necessarily clocked) execute instructions in parallel (*see* "PARALLEL PROCESSOR SYSTEM" as

shown at the top of Figure 1). See also line 1 of Motomura's Abstract: "A parallel processor system executing a program consist[ing] of a plurality of threads in parallel . . . ." *See In re Schreiber* at 1477 (Fed. Cir. 1997) (The absence of a disclosure relating to function does not defeat a finding of anticipation if all the claimed structural limitations are found in the reference).

On this record, we conclude that Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's rejection of representative claim 1 (and claims 2-7, 10-12, 14-20, 23-25, 27-33, 36-38, and 41 that fall therewith) as being anticipated by Motomura.

Dependent claim 8

We consider the Examiner's rejection of representative claim 8 as being anticipated by Motomura. Claim 8 recites "[t]he apparatus of claim 1 wherein the processing slice disables the first thread after sending the command message if the command message is a wait instruction."

Appellants contend that Motomura does not overcome the deficiencies previously argued regarding claim 1. In response, we see no deficiencies regarding the Examiner's rejection of claim 1 as being anticipated by Motomura, as discussed *supra*.

However, Appellants further note that Motomura discloses that a possible reason for a thread to enter the waiting state "is to read data in the

memory in another processor or because of a failure of synchronizing operations." (Motomura, col. 1, 11. 36-39) (App. Br. 15, ¶1).

Thus, Appellants contend that the Examiner has erred because Motomura's ordered multithread executing system cannot also be the peripheral unit to which command messages are sent, while those command messages simultaneously cause a thread to be disabled by a processing slice (App. Br. 15, §2).

In response, we note again that during the Hearing conducted on July 9, 2008, Appellants' representative Edward J. Kessler acknowledged that it was reasonable that a peripheral unit was inherently coupled to the parallel processor system of Motomura, as discussed *supra*.

Therefore, we see no error in the Examiner's reasoning. Moreover, the Examiner has pointed to Motomura's waiting state as disabling a thread (col. 8, ll. 40-42) (Ans. 5). On this record, we conclude that Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's rejection of representative claim 8 (and claims 9, 21, 22, 34, and 35 that fall therewith) as being anticipated by Motomura.

Obviousness under 35 U.S.C. § 103

PRINCIPLES OF LAW

"What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under *§ 103*." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id.* at 1740. Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)). Therefore, we look to Appellants' Briefs to show error in the proffered prima facie case.

Claims 13, 26, and 39

We consider the obviousness rejection of claims 13, 26, and 39 that stand rejected as being unpatentable over Motomura in view of Hiraoka.

Appellants contend that each of claims 13, 26, and 39 are allowable for the same reasons previously argued regarding independent claims 1, 14, and 27 respectively (App. Br. 16-17).

In response, we see no deficiencies with the Examiner's rejection of claims 1, 14, and 27, as being anticipated by Motomura, as discussed *supra*. Therefore, we conclude that Appellants have not shown the Examiner erred in rejecting claims 13, 26, and 39 as being unpatentable over Motomura in view of Hiraoka.

Independent claim 40

We consider next the Examiner's rejection of independent claim 40 as being unpatentable over Motomura in view of Hiraoka and Dove.

Appellants contend that independent claim 40 is allowable for the same reasons previously argued regarding independent claim 1 (App. Br. 17).

In response, we see no deficiencies with the Examiner's rejection of claim 1 as being anticipated by Motomura, as discussed *supra*.

Appellants further contend that neither Motomura, Hiraoka, or Dove teaches or suggests a plurality of peripheral units, as required by independent claim 40 (App. Br. 17). Appellants also contend that "[t]he Examiner does not indicate where the missing teaching of a 'plurality of peripheral units' may be found in either reference, such as may be coupled over a peripheral bus to transfer peripheral information" (App. Br. 18).

In response, we note again that during the Hearing conducted on July 9, 2008, Appellants' representative Edward J. Kessler acknowledged that it was reasonable that a peripheral unit was inherently coupled to the parallel

processor system of Motomura, as previously discussed. We agree and find that an artisan would have concluded as a matter of common sense that a single peripheral unit would have at least suggested connecting plural peripheral units to a computer system, such as that disclosed by Motomura. "Rigid preventative rules that deny factfinders recourse to common sense, however, are neither necessary under our case law nor consistent with it." *KSR* at 1742-43.

Moreover, Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR* at 1734. Here, we find that connecting plural peripheral units to a computer system would have been an obvious modification to an artisan possessing ordinary skill and common sense.

On this record, we conclude that Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's rejection of independent claim 40 as being unpatentable over Motomura in view of Hiraoka and Dove.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude Appellants have not met their burden of showing that the Examiner erred in

rejecting claims 1-12, 14-25, 27-38, and 41 under 35 U.S.C. § 102(b) for anticipation.

Likewise, we conclude Appellants have not met their burden of showing that the Examiner erred in rejecting claims 13, 26, 39, and 40 under 35 U.S.C. § 103(a) for obviousness.

Therefore, claims 1-41 are not patentable.

DECISION

We affirm the Examiner's decision rejecting claims 1- 41.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON DC 20005